Interconnection Arch for RISC-V based SoC FPGA

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@Hercules-Micro

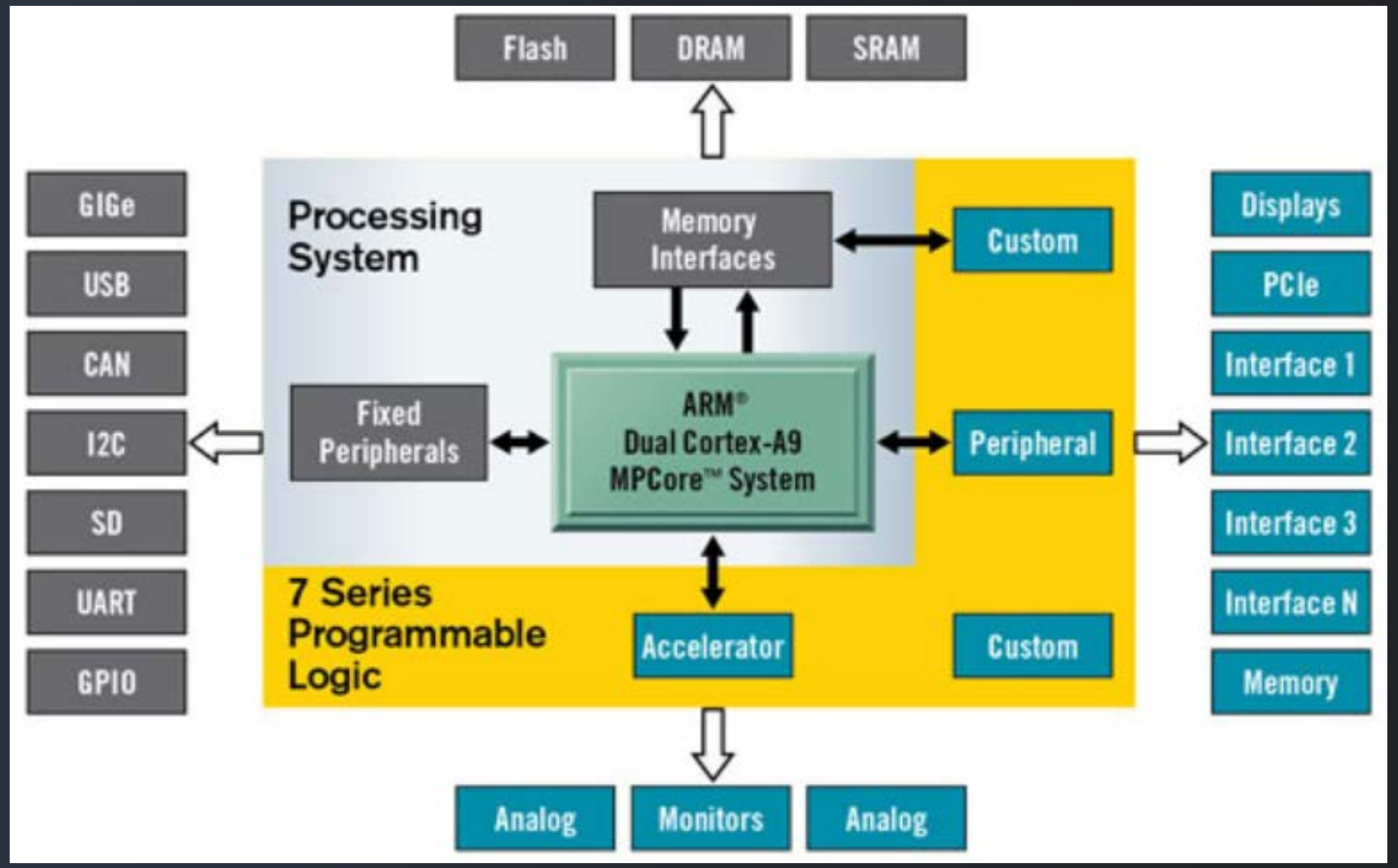
Overview

- Hercules-Micro is leading FPGA architecture and chip innovator, based in Beijing, China

- This slide show our early research on chip2chip/DIE2DIE interconnection arch of RISC-V based SoC FPGA in single-digit process IC manufacturing and AI accelerating era

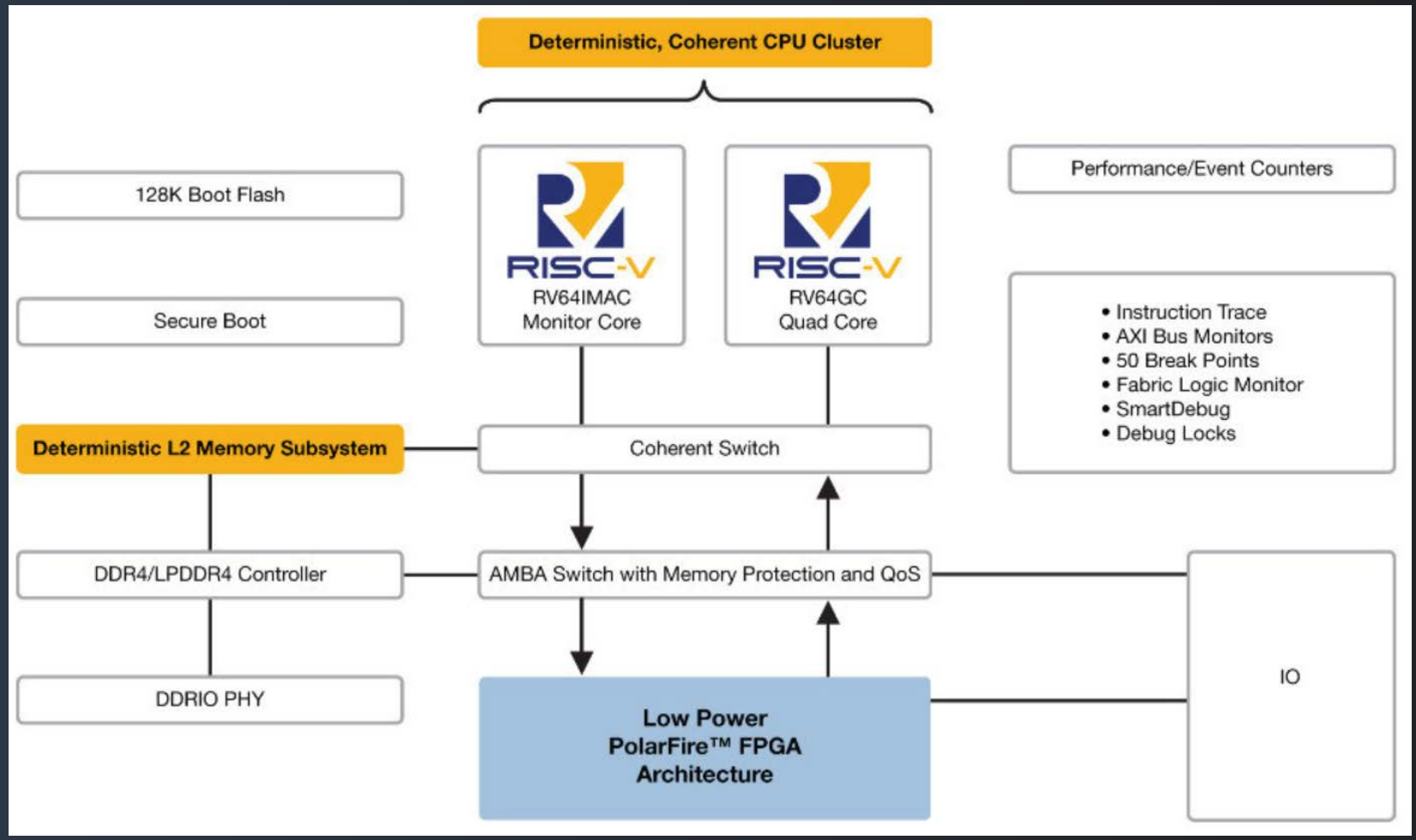
SoC FPGA

- Xilinx Zynq SoC FPGA
- Dual core Cortex-A9
- 28nm FPGA
- Single DIE
- AMBA bus switch



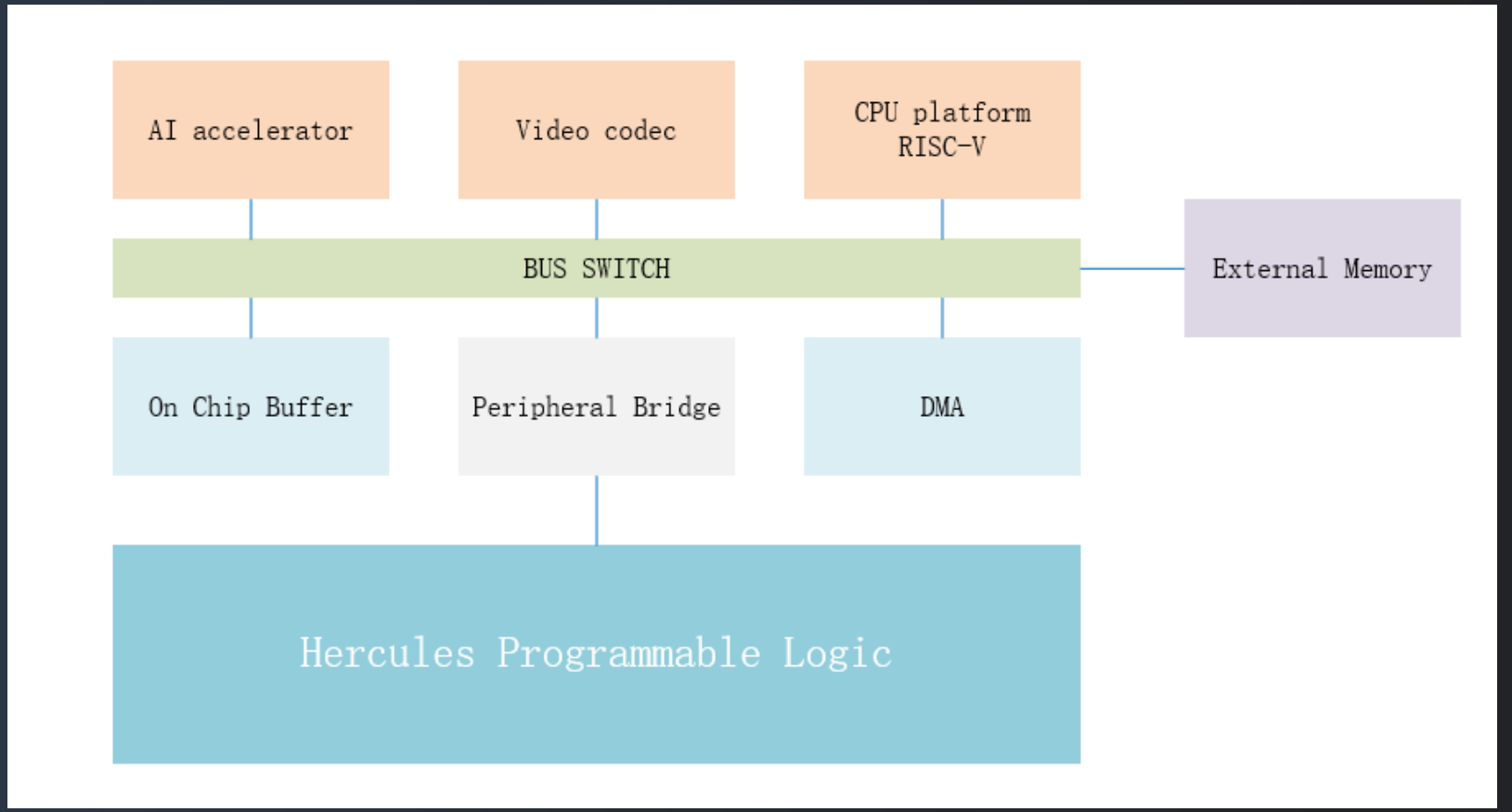
RISC-V inside

- Microsemi PolarFire
- Quadcore RISC-V
  - SiFive U54-MC
- 28nm FPGA
- Single DIE
- AMBA bus switch

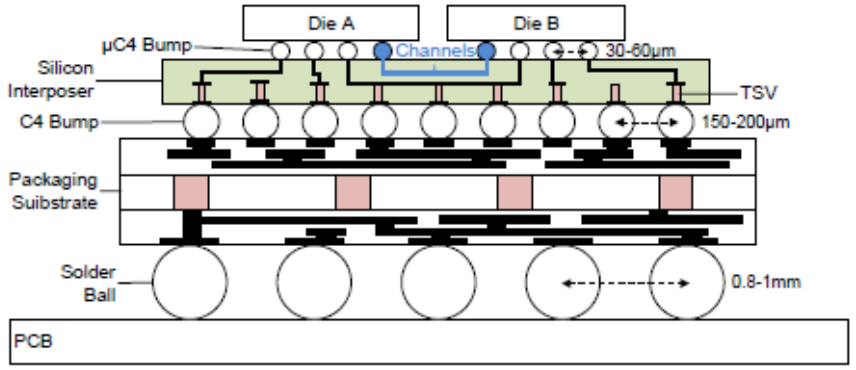


Hercules SoC FPGA

- RISC-V quad core
- AI accelerator inside
- Multi DIE, diff process
- AMBA/TileLink bus

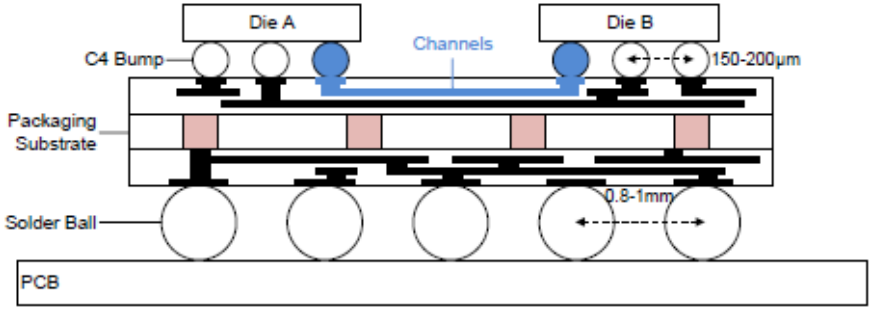


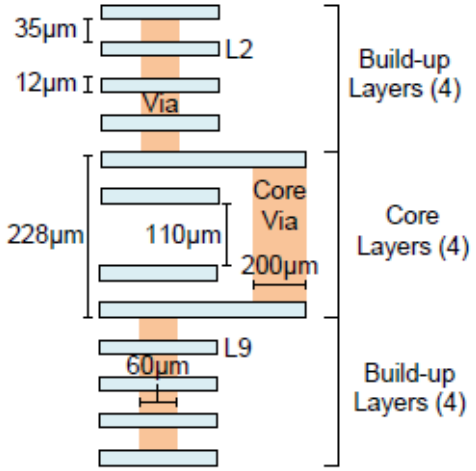
2.5D package



Top: multi-die package with Si interposer;

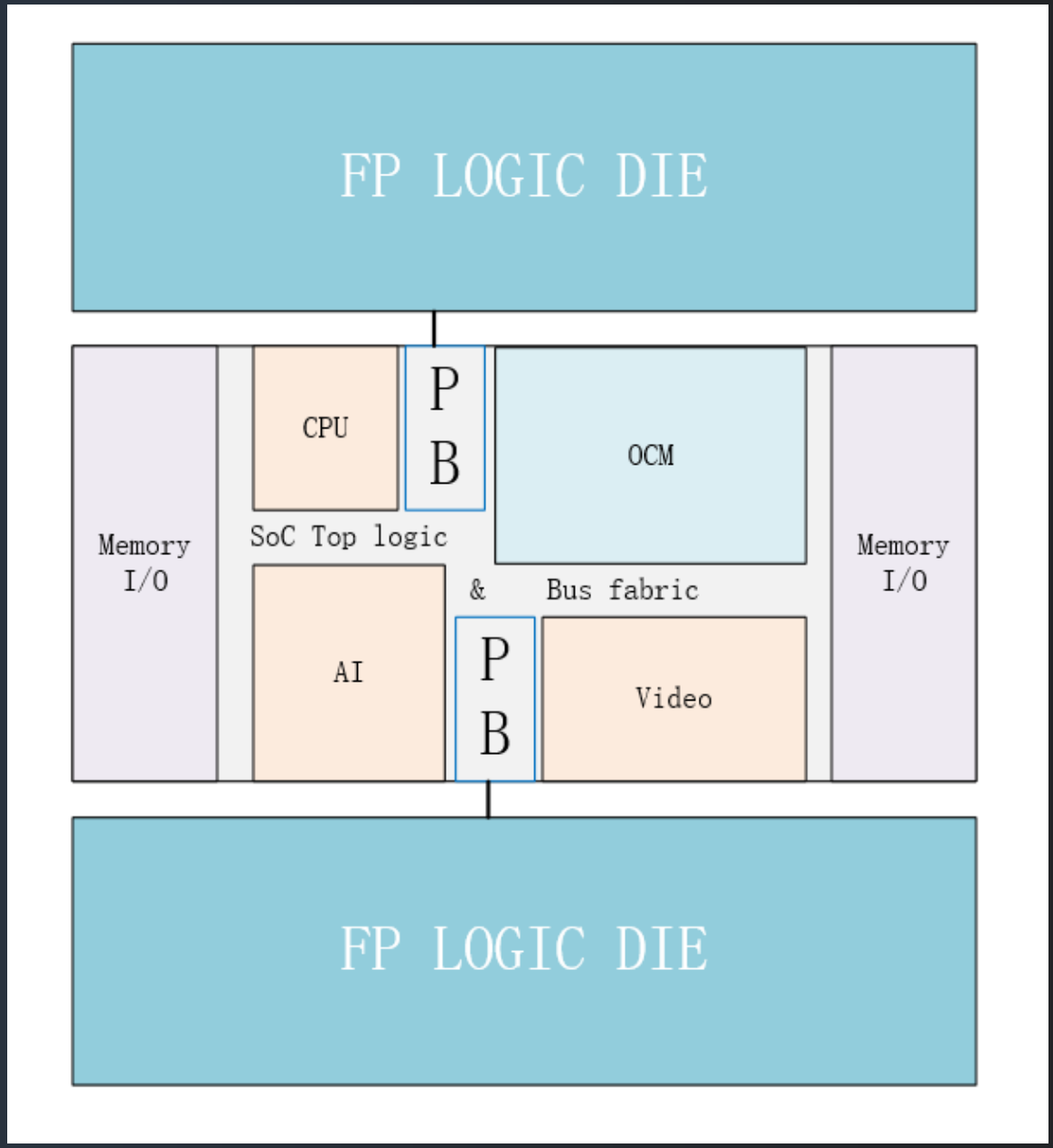
Bottom: multi-die directly on organic substrate, with substrate cross-section





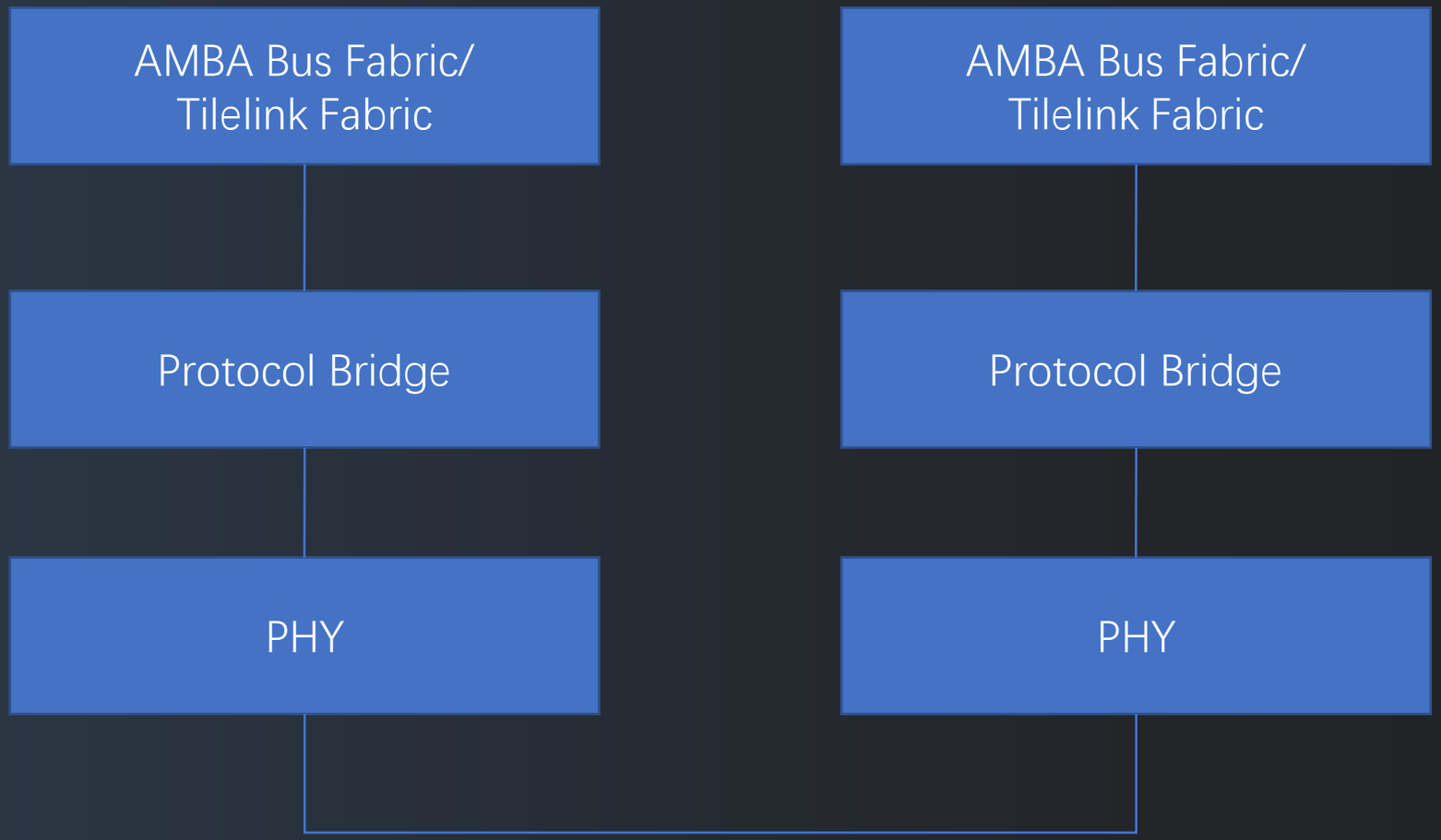
Chip planning

- single/double side FP DIEs
- FP DIE 40nm/22nm/16nm process
- SoC DIE 28nm/12nm/7nm process
- multi combination



PB interface

- High bandwidth
- ChipLink(TileLink)
- PCIe
- Aurora
- AIB
- USR D2D



TileLink (tilelink_spec_1.8.1)

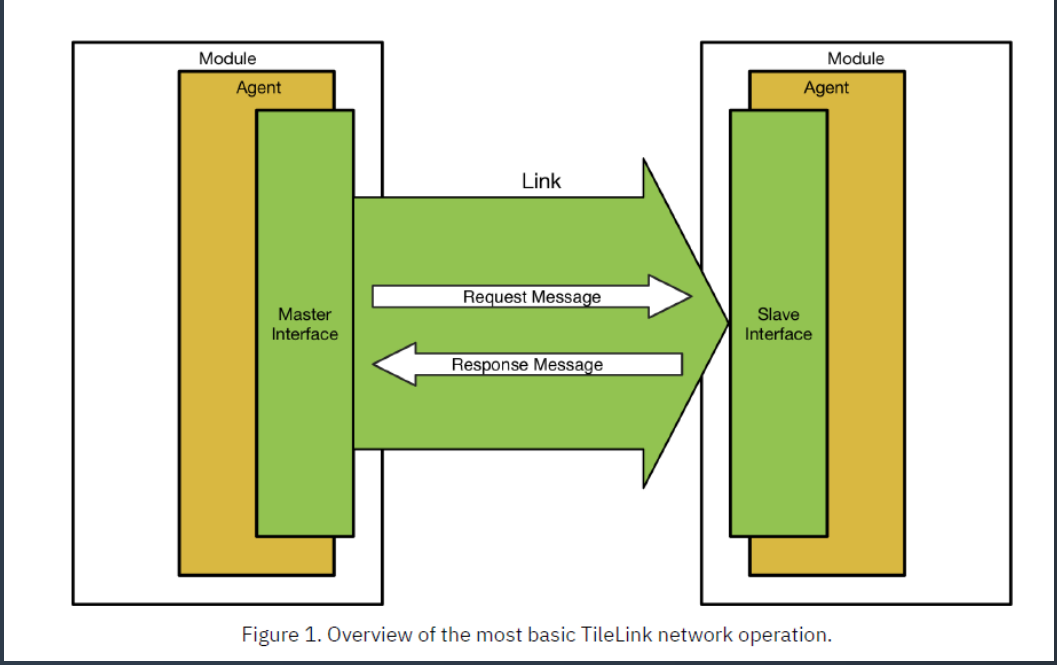


Figure 1. Overview of the most basic TileLink network operation.

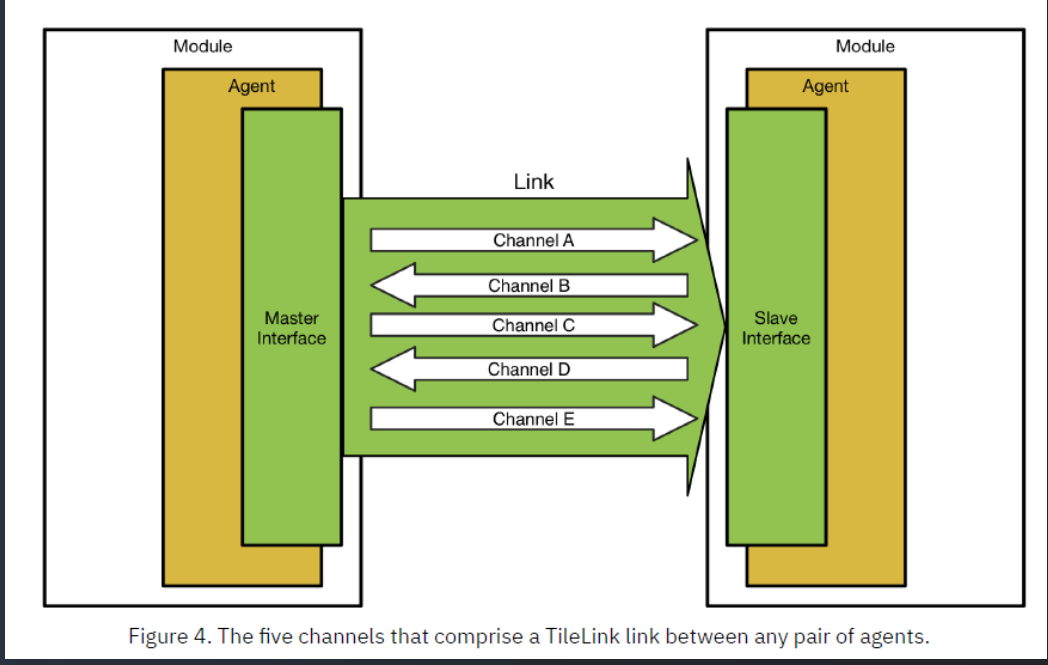
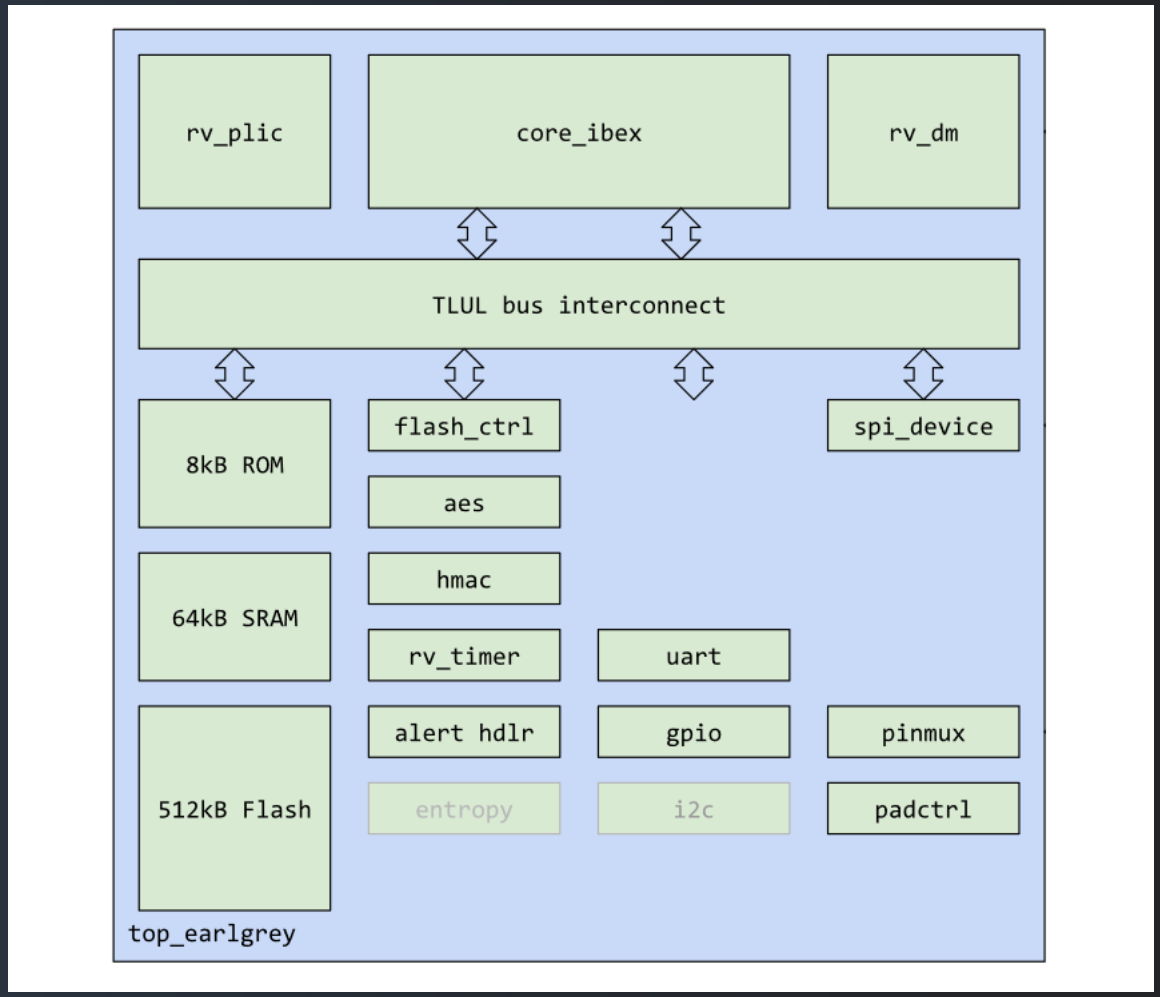


Figure 4. The five channels that comprise a TileLink link between any pair of agents.

Tilelink agents move data in messages across a link: Put, Get, AccessAck, AccessAckData

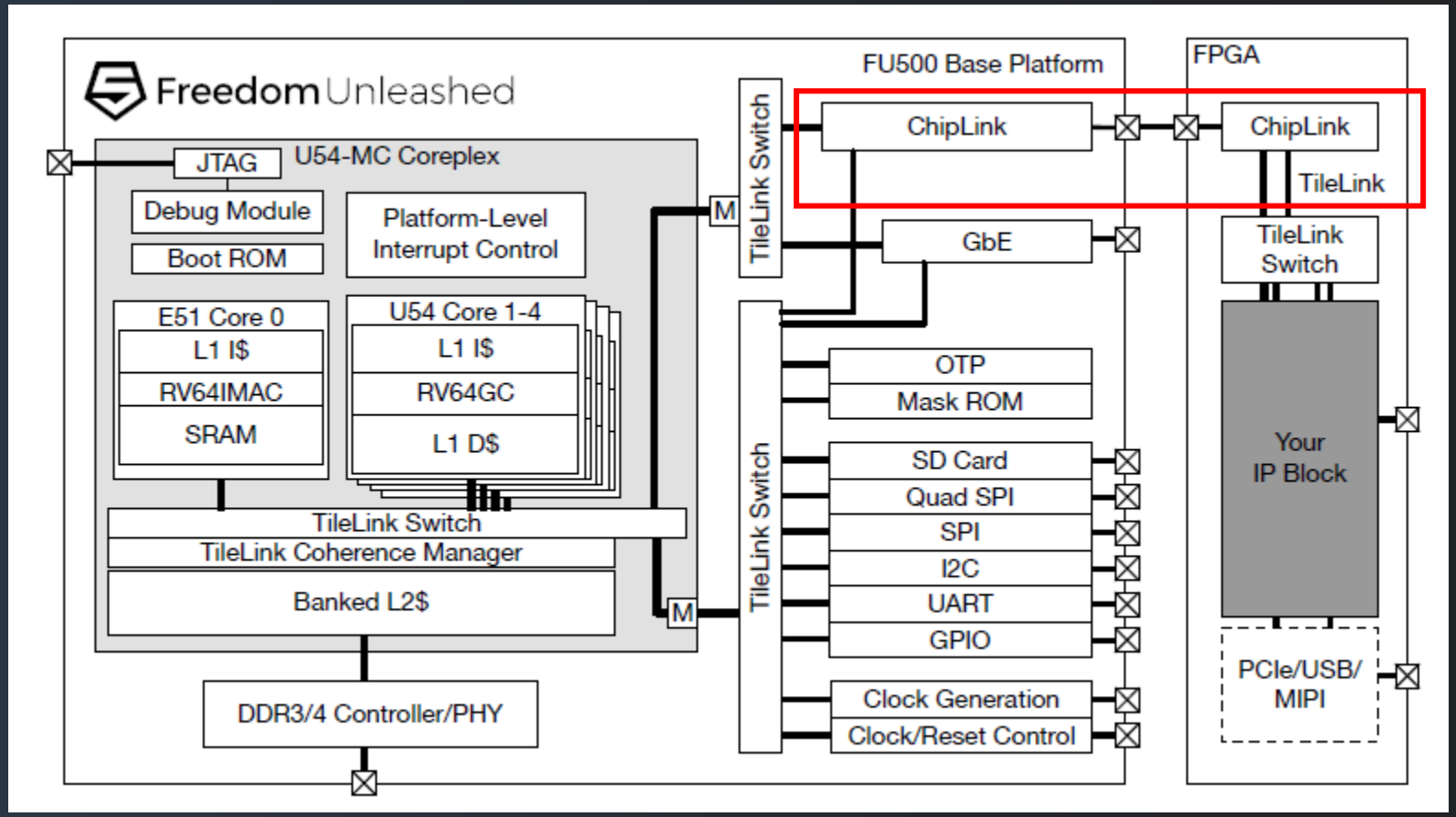
Google OpenTitan: TL-UL

- TL-UL
  - TileLink Uncached Lightweight
- On par of pincount with APB but with the transaction performance of AXI-4



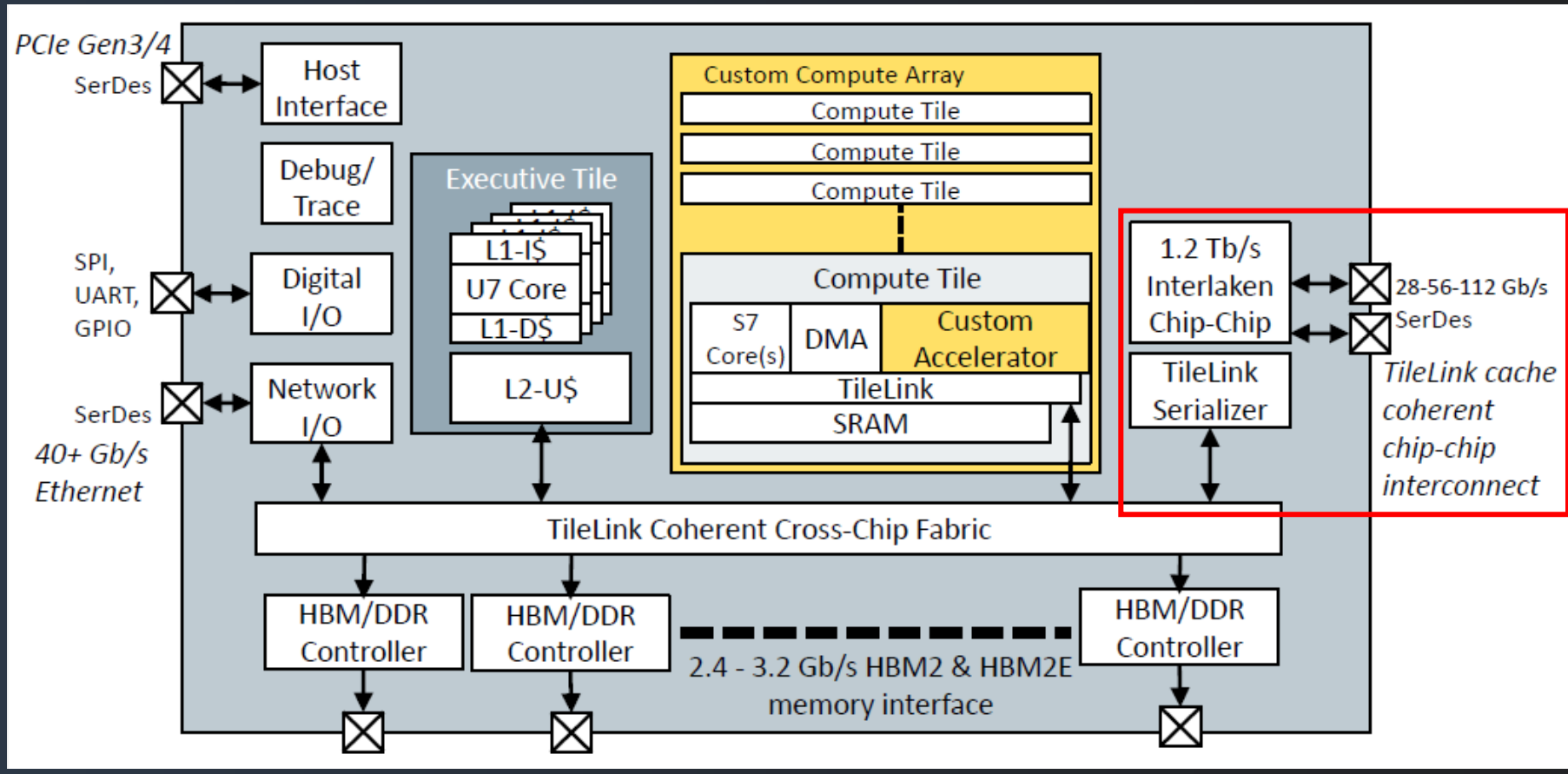
Chip2chip Reference

- 28nm Freedom U500
- TileLink based switch
- ChipLink
  =Serialized TileLink
- SiFive Proprietary



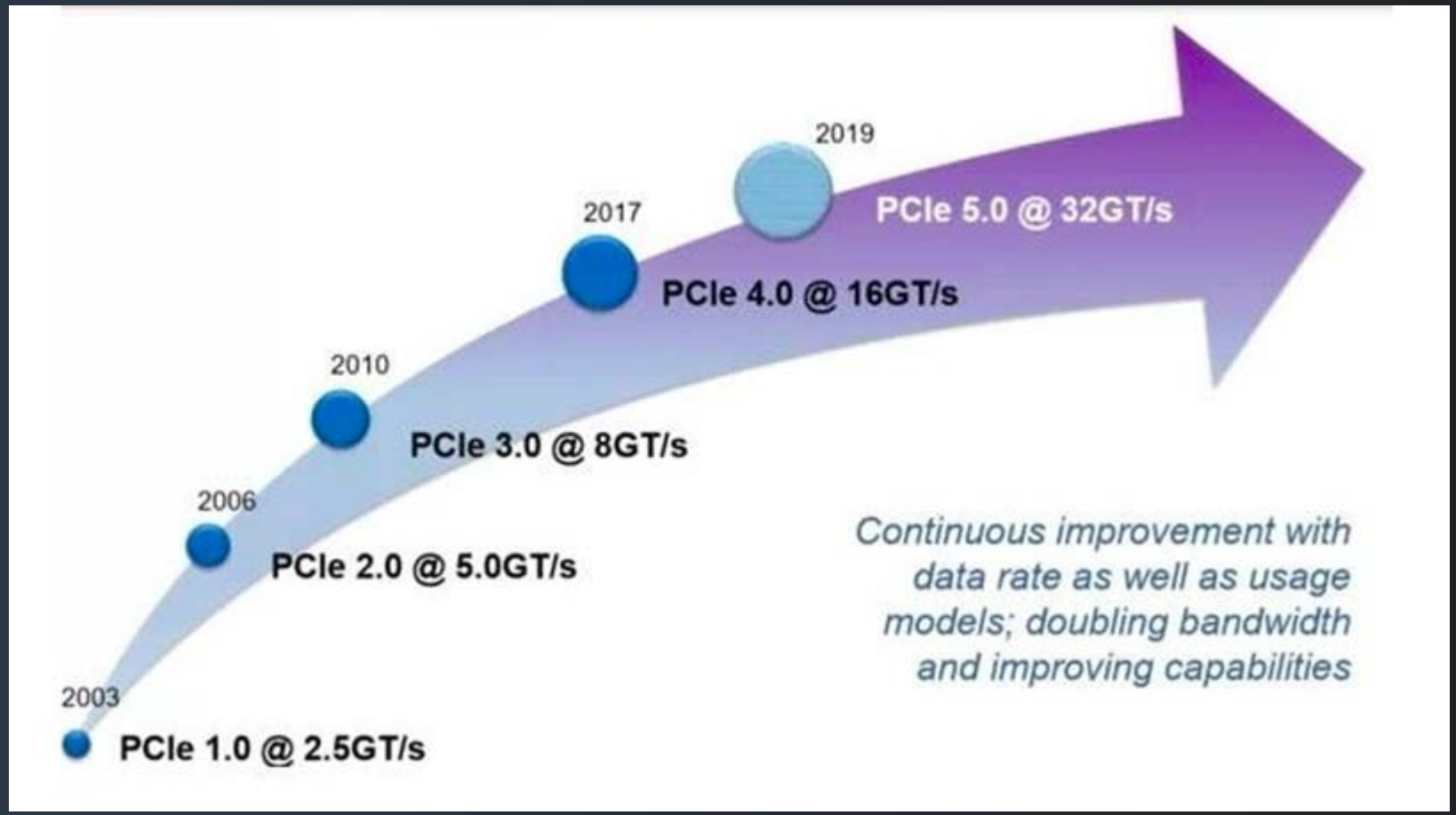
TileLink over Interlaken

- Freedom Evolution
- 16nm/7nm
- up to 1.2Tb/s with 24 lanes x 56Gb/s



PCIe

- Industry standard
- Complex protocol
- AMBA-PCIe bridge



Aurora

- Xilinx's open protocol
- 64b/66b
- up to 25.78 Gb/s single lane
- 400 Gb/s on x16 lanes
- Simple protocol

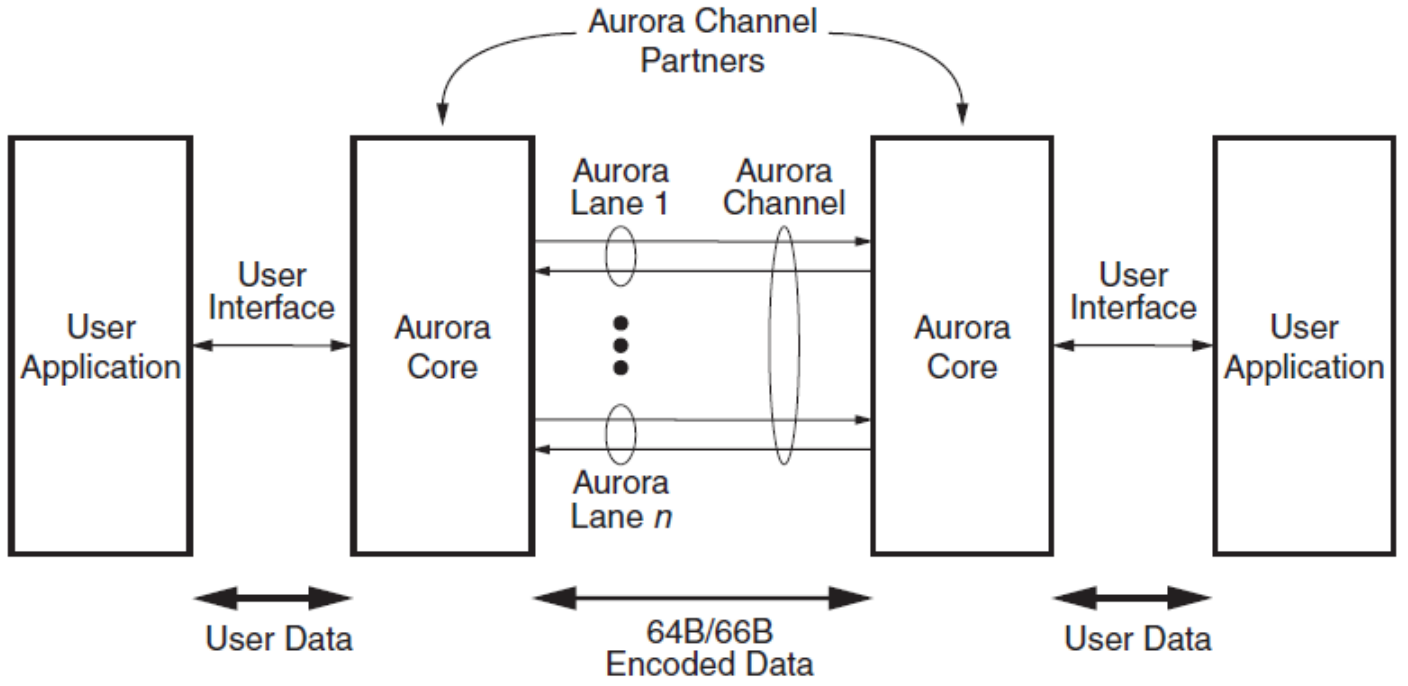
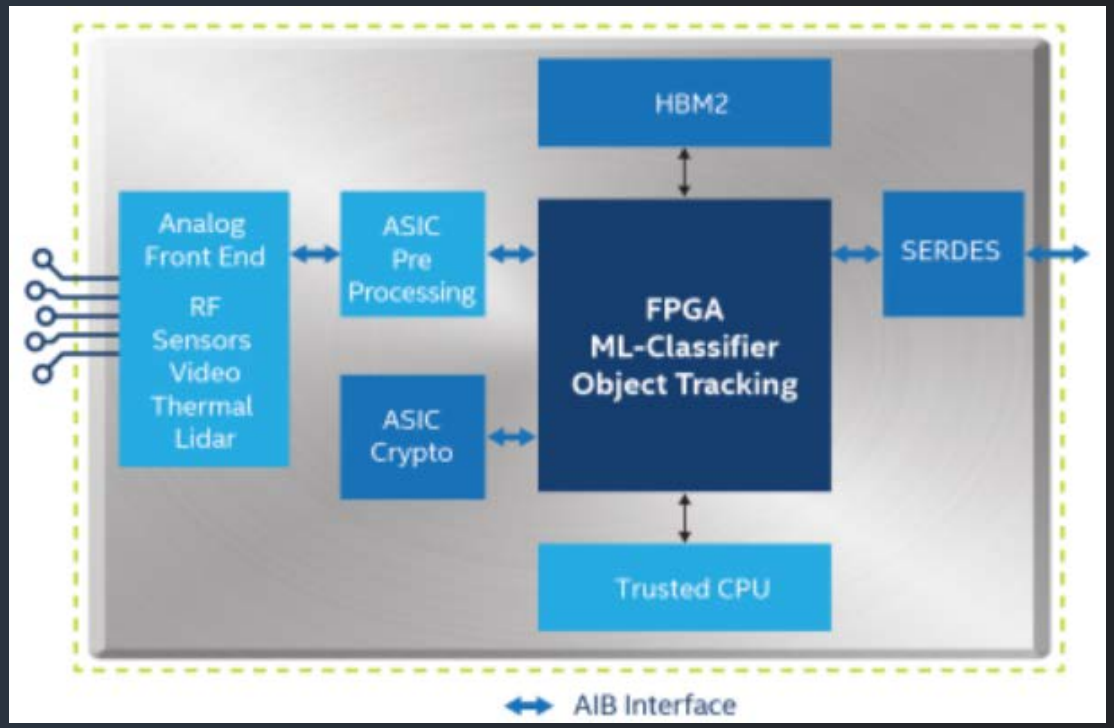


Figure 1-1: **Aurora Protocol Overview**

AIB

- Intel's open source protocol and IP
- AIB = Advanced Interface Bus
- Dedicated for Ultra-Short Reach Die-Die interconnection < 10mm
- Wide signals as HBM



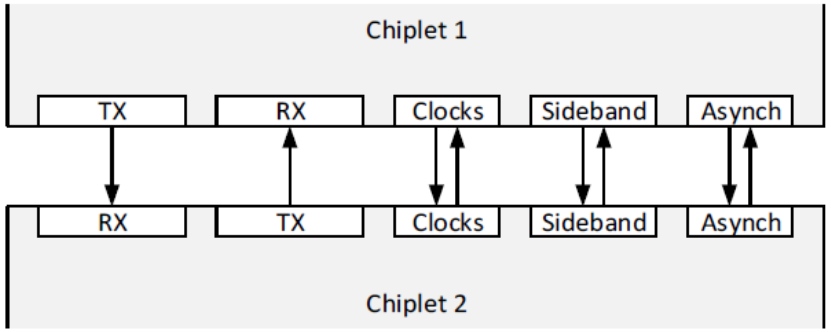


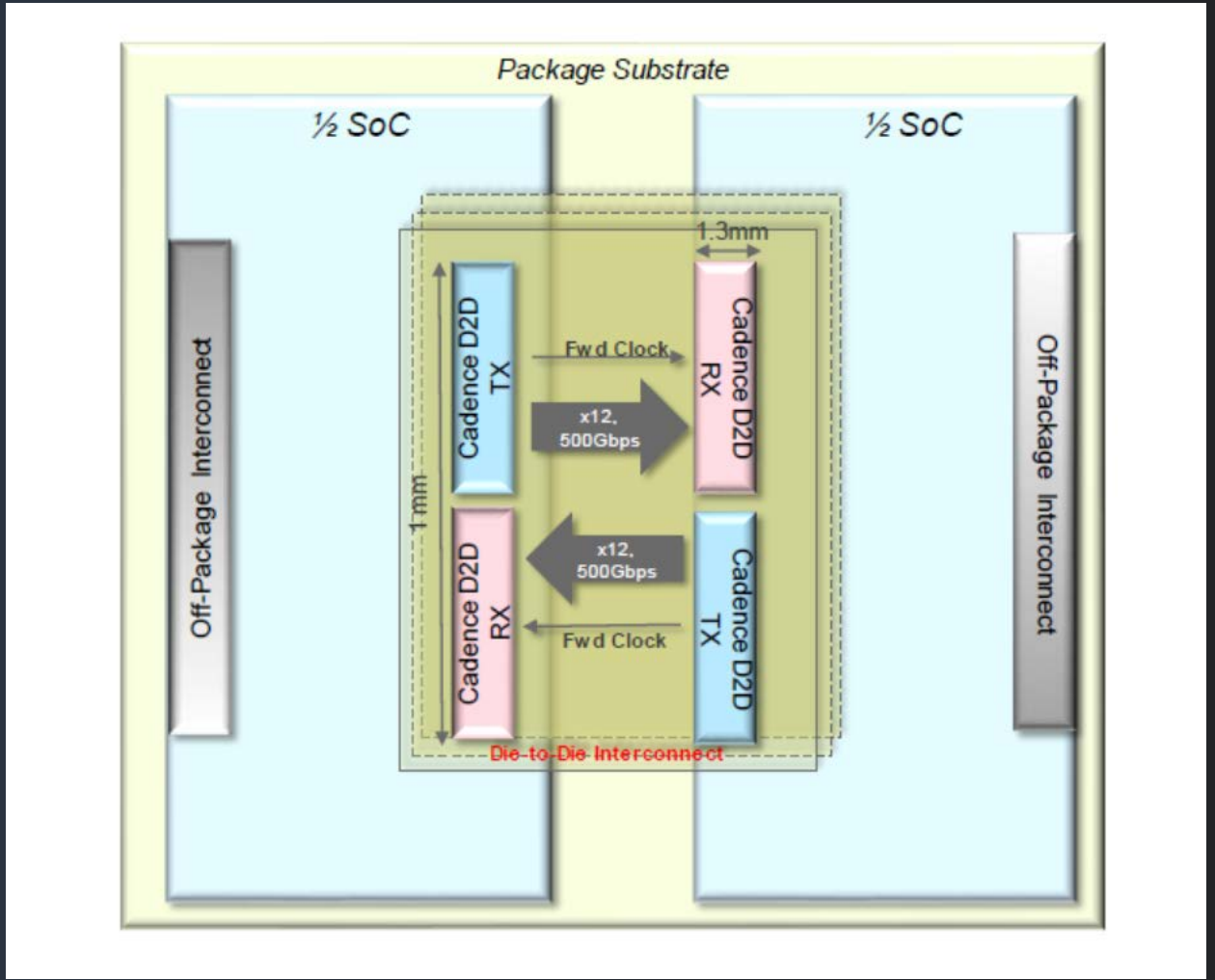
Figure 5. AIB Signal Types

Configuration	Clock/data relationship	Minimum Operating Clock Rate	Minimum Operating Data Rate
AIB Base	SDR	≤ 1 GHz	≤ 1 Gbps
AIB Plus	SDR	≤ 1 GHz	≤ 1 Gbps
	DDR	≤ 1 GHz	≤ 2 Gbps

Table 2. Clock and Data Rates

USR D2D PHY

- D2D dedicated
- Clock forwarded
- no CDR and FEC needed
- NRZ rather PAM4
- High power, Low latency
- up to 40G per lane



Future work

- Power analysis of each method
- Floorplan and PR analysis of each method

- Find me if any questions or suggestions:
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  - Wechat: 18612186995

- The END